REMARKS/ARGUMENTS

Figures 3 and 4 have been amended such that Figures 3 and 4 be consistent with the detailed description of the application.

Claim rejections
35 USC § 112

Claims 2 and 16 were rejected under 35 U.S.C. 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. The Applicant has amended Claims 2 and 16 in order to overcome this rejection.

Claim rejections
35 USC § 102

Claims 1-2, 5-11, 13-16 and 18-20 were rejected under 35 USC 102(b) as being allegedly anticipated by Coker U.S. Pat. No. 5,371,878 (hereinafter, Coker). The Applicant respectfully traverses the rejection.

Independent Claim 1 recites (emphasis added):

"A system for debugging microcontroller code comprising:

a microcontroller ...;

an ICE (in circuit emulator) ..., wherein the ICE emulates the microcontroller, the microcontroller and the ICE run the microcontroller code in lock step; and

an interface for coupling the test circuit and the ICE enabling data transmission between the test circuit and the computer system, the computer

system configured to compare a content of the first memory against a content of the second memory to verify said lock step."

The rejection relies on the target-ECS 12 connected to the system hardware 16 in order to show a microcontroller installed on a test circuit as claimed. The rejection relies on ICE 32 in order to show ICE (in circuit emulator), as claimed. The rejection further relies on a shadow system 28 executing the same software and input signals as the target-ECS 12 to show ICE emulating the microcontroller. (See Coker, col. 4, lines 40-43). As such, it is the shadow system 28 that emulates the target-ECS 12 by executing the same software and not the ICE 32 as disclosed.

Independent Claim 1 distinguishes over Coker by reciting the limitation that the ICE emulates the microcontroller. Coker on the other hand fails to show ICE emulating the microcontroller but rather discloses a shadow system 28, which differs from the ICE, emulating the target-ECS 12 by executing the same software and input signals as the target-ECS 12. Accordingly, Coker does not disclose ICE emulates the microcontroller, as claimed.

Moreover, Coker discloses that a shadow system 28 is connected to an ICE 32 via an electrical connection and that by operating on input data with the same value, memory location and relative timing as the target-ECS, the shadow system has an execution state at any given time corresponding to a known execution state in the target-ECS, however, the shadow system is not an ICE as claimed. (See Coker, col. 4, lines 51-52 and col. 3, lines 6-12). As such, Coker

teaches a target-ECS and the shadow system operating on input data with the same value, memory location and relative timing of one another.

Independent Claim 1 distinguishes over Coker by reciting that the ICE runs the microcontroller code in lock step. On the other hand Coker discloses a target-ECS and the shadow system operating on input data with the same value, memory location and relative timing of one another. Accordingly, Coker does not disclose that the ICE runs the microcontroller code in lock step, as claimed.

Moreover, independent Claim 1 distinguishes over Coker by reciting that the computer system is configured to compare a content of the first memory against a content of the second memory to verify said lock step. As discussed above Coker discloses that by operating on input data with the same value, memory location and relative timing as the target-ECS, the shadow system has an execution state at any given time corresponding to a known execution state in the target-ECS. The Applicant has found no teaching in Coker suggesting comparison of memories to verify the lock step as claimed. Accordingly, Coker does not disclose the computer system configured to compare a content of the first memory against a content of the second memory to verify said lock step, as claimed.

Therefore, Coker does not disclose the limitation that the ICE emulates the microcontroller, neither does Coker disclose that the ICE runs the microcontroller code in lock step, nor does Coker disclose the computer system configured to

compare a content of the first memory against a content of the second memory to verify said lock step, as claimed. Thus, Coker does not disclose the limitations of the claimed invention. Accordingly, independent Claim 1 is not anticipated by Coker under 35 U.S.C. 102(b). Claims 2 and 5-8 depend from independent Claim 1 and are therefore patentable over Coker at least for the same reasons that Claim 1 is patentable. As such, allowance of Claims 1-2 and 5-8 is earnestly solicited.

Independent Claim 15 is similar in scope to that of independent Claim 1 and is therefore not anticipated by Coker under 35 U.S.C. 102(b) at least for the same reasons that independent Claim 1 is patentable. Claims 16 and 18-20 depend from independent Claim 15 and are each patentable under 35 U.S.C. 102(b) at least for the same reasons that independent Claim 15 is patentable.

Moreover, Claim 16 is similar in scope to that of Claim 2 and is patentable at least for the same reasons that Claim 2 is patentable as discussed above.

As such, allowance of Claims 15-16 and 18-20 is earnestly solicited.

Independent Claim 9 is similar in scope to that of independent Claim 1 and is therefore not anticipated by Coker under 35 U.S.C. 102(b) at least for the same reasons that independent Claim 1 is patentable. Claims 10-11 and 13-14 depend from independent Claim 9 and are each patentable under 35 U.S.C. 102(b) at

least for the same reasons that independent Claim 9 is patentable. As such, allowance of Claims 9-11 and 13-14 is earnestly solicited.

Claim rejections
35 USC § 103

Claims 3, 12 and 17 were rejected as being allegedly unpatentable under 35 U.S.C. 103(a) over Coker in view of Barnett (U.S. Patent No. 6,173,419) (hereinafter Barnett). The Applicant respectfully traverses the rejections.

Claims 3, 12 and 17 depend from independent Claims 1, 9 and 15 respectively. As such, Claims 3, 12 and 17 include the limitations of their independent Claims respectively. As discussed above, Coker does not disclose the limitation that the ICE emulates the microcontroller, neither does Coker disclose the limitation that the ICE runs the microcontroller code in lock step, nor does Coker disclose the computer system configured to compare a content of the first memory against a content of the second memory to verify said lock step, as claimed. The Applicant does not understand Barnett to remedy these defects. Accordingly, the combination of Coker and Barnett does not teach the limitations of Claims 3, 12 and 17. Thus, the combination of Coker and Barnett does not render Claims 3, 12 and 17 obvious under 35 U.S.C. 103(a). As such, allowance of Claims 3, 12 and 17 is earnestly solicited.

Claim 4 was rejected as being allegedly unpatentable under 35 U.S.C. 103(a) over Coker in view of "State of the Art" by Stan Augarten, published 1983 (Augarten). The Applicant respectfully traverses the rejection.

Claim 4 depends from independent Claim 1. As such, Claim 4 includes the limitations of independent Claim 1. As discussed above, Coker does not disclose the limitation that the ICE emulates the microcontroller, neither does Coker disclose the limitation that the ICE runs the microcontroller code in lock step, nor does Coker disclose the computer system configured to compare a content of the first memory against a content of the second memory to verify said lock step, as claimed. The Applicant does not understand Augarten to remedy these defects. Accordingly, the combination of Coker and Augarten does not teach the limitations of Claim 4. Thus, the combination of Coker and Augarten does not render Claim 4 obvious under 35 U.S.C. 103(a). As such, allowance of Claim 4 is earnestly solicited.

For the above reasons, the Applicant requests reconsideration and withdrawal of these rejections under 35 U.S.C. 102(b), 35 U.S.C. 112 and 35 U.S.C. §103.

CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims 1-20 is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-20 overcome the rejections of record and, therefore, allowance of Claims 1-20 is earnestly solicited.

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Respectfully submitted,
WAGNER, MURABITO & HAO LLP

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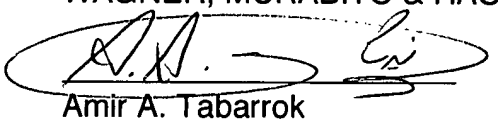

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